IN THE CLAIMS

1. (Currently amended) System comprising:

_____ a first processor bus ~~(10; 70; 90)~~,

_____a first processor ~~(P1) being connectable~~coupled to the first processor bus ~~(10; 70; 90)~~,

_____a first direct memory access unit ~~(45; 83; 101)~~ with a first external direct memory access channel ~~(47; 85; 106)~~, the first direct memory access unit ~~(45; 83; 101)~~ being ~~connectable~~ coupled to the first processor bus ~~(10; 70; 90)~~,

_____a first programmable unit ~~(34; 82; 92) being connectable~~coupled via the first external direct memory access channel ~~(47; 85; 106)~~ to the first direct memory access unit ~~(45; 83; 101)~~, said first programmable unit ~~(34; 82; 92)~~ being programmable by the first processor ~~(P1)~~,

_____a first shareable unit ~~(13; 76; 93) being connectable~~coupled to the first processor bus ~~(10; 70; 90)~~,

_____a second processor bus ~~(20; 80; 100)~~,

_____a second processor ~~(P2) being connectable~~coupled to the second processor bus ~~(20; 80; 100)~~,

_____a second direct memory access unit ~~(35; 73; 93)~~ with a second external direct memory access channel ~~(36; 75; 96)~~, the second direct memory access unit ~~(35; 73; 93)~~ being ~~connectable~~ coupled to the second processor bus ~~(20; 80; 100)~~,

_____a second programmable unit ~~(44; 72; 92) being connectable~~coupled via the second external direct memory access channel ~~(36; 75; 95)~~ to the second direct memory access



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unit ~~(35; 73; 93)~~, said second programmable unit ~~(44; 72; 92)~~ being programmable by the second processor ~~(P2)~~, and

a second shareable unit ~~(23; 86; 103)~~ being connected to the second processor bus ~~(20; 80; 100)~~,

wherein the first programmable unit and the second programmable unit each comprises a processor interface, a direct access unit core, and two external direct memory access channel interfaces,

wherein a first bi-directional communication channel is ~~establishable~~ established between the first shareable unit ~~(13; 76; 93)~~ and the second processor ~~(P2)~~, and a second bi-directional communication channel is ~~establishable~~ established between the second shareable unit ~~(23; 86; 103)~~ and the first processor ~~(P1)~~.

2. (Previously presented) The system of claim 1, wherein the first bi-directional communication channel and/or the second bi-directional communication channel are half-duplex channels or full-duplex channels.

3. (Currently amended) The system of claim 1, wherein the processor ~~(P1)~~ and the processor ~~(P2)~~ are similar from an architectural point of view.

4. (Currently amended) The system of claim 1, wherein the processor ~~(P1)~~ and the processor ~~(P2)~~ are implementations of the same type of processor design.

5. (Currently amended) The system of claim 1, wherein the processor ~~(P1)~~ and the



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processor ~~(P2)~~ are implementations of different types of processor design.

6. (Currently amended) The system of ~~the claims 1-5~~claim 1, wherein the shareable unit ~~(13; 76; 93; 23; 86; 103) is either~~is one of the following: a memory, a peripheral, an interface, an input device, an output device.

7. (Currently amended) The system of ~~the claims 1-5~~claim 1, wherein one of the two integrated processors ~~(P1, P2)~~ is a central processing unit ~~(CPU)~~, a microprocessor, a digital signal processor ~~(DSP)~~, a system controller ~~(SC)~~, a co-processor, or an auxiliary processor.

8. (Canceled)

9. (Currently amended) The system of claim ~~1~~8, wherein the processor interface ~~(50; 60; 110; 120)~~ has a programming link ~~(12, 22; 32, 42; 51, 52; 74, 84; 94, 104)~~ either for connecting to a processor bus ~~(10, 20; 70, 80; 90, 100)~~ or for connecting to a processor ~~(P1, P2)~~.

10. (Currently amended) The system of ~~any of the preceding claims~~claim 1, wherein ~~the communication channels are establishable for transferring~~ data and/or control information is transferred to and from the shareable unit ~~(13; 76; 93; 23; 86; 103)~~via the communication channels.



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11.-12. (Canceled)



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